TSMC-01-195CC

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May 11, 2004

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572 28 Davis Avenue Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/823,149 04/13/04

Lain-Jong Li et al.

COMPOSITE ETCHING STOP IN SEMI-CONDUCTOR PROCESS INTEGRATION

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

## CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 17, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

## TSMC-01-195CC

- U.S. Patent 6,127,262 to Huang et al., "Method and Apparatus for Depositing an Etch Stop Layer," discloses a process for an etch stop layer.
- U.S. Patent 6,209,484 to Huang et al., "Method and Apparatus for Depositing an Etch Stop Layer," discloses a process for an etch stop layer.
- U.S. Patent 5,585,304 to Hayashi et al., "Method of Making Semiconductor Device with Multiple Transparent Layers," discusses a semiconductor wafer which is comprised of a transparent layer interposed between a thin silicon layer and a thick silicon layer.

Sincerely,

Stephen B. Ackerman,

Reg. No. 37761

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